Verilog code 파일명 : segment.v

`timescale 1ns / 1ps

module segment(

input a,b,c,d, output A,B,C,D,E,F,G,seg);

assign A = (b&c) | (!a&c) | (a&!d) | (!b&!d) | (!a&b&d) | (a&!b&!c);

assign B = (!b&!d) | (!b&!c) | (!a&c&d) | (a&!c&d) | (!a & !c & !d);

assign C = (!c & d) | (!a & d ) | (a & !b) | ( !a & b) | (!b & !c);

assign D = (!a &c & !d) | (!b & c & d) | (b & !c & d) | ( a &b&!d) | (!b&!c&!d);

assign E = (c &!d) | (a &c) | (a&b) | (!b & !d);

assign F = (a & c ) | (a&!b) | (b&!d) | (!c&!d) + (!a&b&!c);

assign G = (a&c) | (!b&c) | (a&!b) | (b&!c&d) | (!a&b&!d);

assign seg =1;

endmodule

simulation code 파일명 : segment\_sim.v

`timescale 1ns / 1ps

module segment\_sim();

reg clk,a,b,c,d;

wire A,B,C,D,E,F,G;

segment connect(

.a(a), .b(b), .c(c), .d(d),

.A(A), .B(B), .C(C), .D(D), .E(E), .F(F), .G(G)

);

initial begin

clk = 0 ; a = 0 ; b = 0 ; c = 0; d = 0;

end

always clk = #10 ~clk;

always @(posedge clk)begin

d<= ~d;

c <= #40 ~c;

b <= #80 ~b;

a <= #160 ~a;

end

endmodule

xdc segment\_c.xdc

set\_property IOSTANDARD LVCMOS18 [get\_ports a]

set\_property IOSTANDARD LVCMOS18 [get\_ports b]

set\_property IOSTANDARD LVCMOS18 [get\_ports c]

set\_property IOSTANDARD LVCMOS18 [get\_ports d]

set\_property IOSTANDARD LVCMOS18 [get\_ports A]

set\_property IOSTANDARD LVCMOS18 [get\_ports B]

set\_property IOSTANDARD LVCMOS18 [get\_ports C]

set\_property IOSTANDARD LVCMOS18 [get\_ports D]

set\_property IOSTANDARD LVCMOS18 [get\_ports E]

set\_property IOSTANDARD LVCMOS18 [get\_ports F]

set\_property IOSTANDARD LVCMOS18 [get\_ports G]

set\_property IOSTANDARD LVCMOS18 [get\_ports seg]

set\_property PACKAGE\_PIN J4 [get\_ports a]

set\_property PACKAGE\_PIN L3 [get\_ports b]

set\_property PACKAGE\_PIN K3 [get\_ports c]

set\_property PACKAGE\_PIN M2 [get\_ports d]

set\_property PACKAGE\_PIN D20 [get\_ports A]

set\_property PACKAGE\_PIN C20 [get\_ports B]

set\_property PACKAGE\_PIN C22 [get\_ports C]

set\_property PACKAGE\_PIN B22 [get\_ports D]

set\_property PACKAGE\_PIN B21 [get\_ports E]

set\_property PACKAGE\_PIN A21 [get\_ports F]

set\_property PACKAGE\_PIN E22 [get\_ports G]

set\_property PACKAGE\_PIN E14 [get\_ports seg]